CORRELATION DETECTOR AND COMMUNICATION APPARATUS

TECHNICAL FIELD

The present invention relates to a correlation detector of a radio receiver in a CDMA (Code Division Multiple Access) system which carries out multiple access by using a spread spectrum in mobile communications.

In particular, the present invention relates to a CDMA synchronizing circuit that synchronizes a spreading code for despreading the received signal to a spreading code in a received signal in CDMA communications.

BACKGROUND ART

CDMA communications perform multiple access propagation by spreading information into wideband signals using spreading codes with rates higher than the rate of the information, and are roughly divided into direct sequence (DS) systems that spread modulated signals by high rate spreading codes, and frequency hopping (FH) systems. The FH system resolves each symbol into smaller elements called chips, and translates the chips into signals with different center frequency at a high speed. Since the implementation of the FH system is difficult, the DS system is generally used. The DS system recovers the original narrowband signal by despreading the wideband received input signal at a receiving end, followed by demodulation. In the despreading process, correlation detection is performed between the spreading code included in the received signal and a spreading code generated at the receiving end.

Thus, the receiver for receiving the spread signal in the DS system is usually provided with a replica (reference PN sequence) of the PN sequence (received PN sequence) in the received signal, and establishes synchronization between the reference PN sequence and the received PN sequence. FIG. **1** shows a conventional synchronization circuit using a matched filter. The received signal applied to an input terminal **10** is supplied to a memory circuit **11** with taps. The number of taps of the tapped memory circuit **11** is the same as the number of chips in a spreading code interval (that is, a processing gain PG). The outputs of the taps of the memory circuit **11** are multiplied by the reference spreading code stored in a tap coefficient circuit **13** by multipliers **12**. The resultant products are summed by an integrator **14**, which outputs the sum from its output terminal **16** as a correlation value **15**.

Using the matched filter makes it possible to quickly establish the synchronization because the peaks of the correlation value appear at the same interval as that of the spreading code. However, since the capacity of the tapped memory circuit **11** and the number of the multipliers **12** increase in proportion to the processing gain, the power consumption of the receiver will increase with the interval of the spreading code. Therefore, the conventional synchronizing circuit is not appropriate for portable devices or mobile devices.

Using a sliding correlation detector as shown in FIG. **2** makes possible power saving and downsizing of the circuit. In FIG. **2**, a received signal **21** inputted to the input terminal **10** is multiplied by a spreading code, which is generated by a spreading code replica generator **30**, by a multiplier **22** to obtain the correlation between the two. The resultant product is passed through a bandpass filter (BPF) **23**, followed by peak power detection by a square-law detector **24**. The detected power is integrated over a fixed time (normally, ± one chip interval) by an integral-dump circuit **25**. The integrated result is compared with a threshold value by a threshold value decision circuit **26** which decides that initial acquisition has been completed if the integrated result exceeds the threshold value, and proceeds to the next step (tracking mode). If the integrated result is less than the threshold value, the decision circuit **26** supplies a control voltage **28** to a voltage controlled clock generator (VCCG) **29** which slides the phase of the replica so that the phase of the spreading code generated by the spreading code replica generator **30** is shifted by 1/N chip interval (N is a natural number equal to or greater than one). The initial acquisition has been completed by repeating the processing until the synchronized point is found.

According to this method, it is necessary to integrate the spreading replica over the fixed time every time the replica is shifted by 1/N chip interval, and to detect the synchronized point in the interval of the spreading code by comparing the integrated result. This will lengthen the acquisition time, and hence, it is not appropriate for a system which requires a quick acquisition.

In addition, the conventional correlation detector presents another problem in that it provides a rather large error in maintaining (tracking) the synchronization.

FIG. **3** is a block diagram showing a conventional DLL (Delay Locked Loop) correlation detector **44**. In FIG. **3**, the same functional blocks are designated by the same numerals as in FIG. **2**. The reference numeral **10** designates a spreaded signal input terminal, **102** designates a decided data output terminal, **111** denotes a multiplier, and **510** designates a delay circuit. The correlation detector **44** calculates correlations between the input modulated signal and code sequences formed by advancing and retarding the chip phase of the replica by 1/N, respectively. The correlated signals are passed through bandpass filters (BPFs) **53** and **54** which eliminate unnecessary high frequency components, and are detected by square-law detectors **55** and **56**. The squared amplitude components are summed by an adder **57** in the opposite phase, so that an error signal voltage is obtained which indicates an amount of a phase difference. The error signal voltage is passed through a loop filter **58**, and is fed back to a VCCG **29** to correct the phase of the replica code sequence. The phase advance (or retardation) time δ ranges from 0 to Tc, where Tc is the chip interval.

Applying the CDMA system to cellular communications requires high accuracy transmission power control that keeps constant base station's received levels of signals sent from all the mobile stations. The CDMA system can increase the capacity in terms of the number of subscribers per frequency band as compared with the FDMA system or the TDMA system. This is because conventional systems which employ frequency orthogonality cannot utilize the same carrier frequencies in the contiguous cells, and even space diversity systems cannot reuse the same frequencies within four cells.

In contrast with this, the CDMA system makes it possible to reuse the same carrier frequency in the contiguous cells because the signals of the other communicators are regarded as white noise. Accordingly, the CDMA system can increase the capacity in terms of the number of subscribers as compared with the FDMA system or the TDMA system. If the processing gain is pg, the number of spreading code sequences that completely orthogonalize with each other is pg. This number of the code sequences, however, will be insufficient when information data is spread by using only code sequences of one symbol interval long. To overcome this problem, the number of the spreading codes is increased